ABSTRACT

Disclosed is a data output buffer having a preset structure. The data output buffer comprises a plurality of groups, each group having two data output buffers, a preset driver for precharging or discharging any one output of two output buffers in each group, a control circuit for generating a control signal to drive the preset driver when outputs of the two output buffers in each group are same, and a set circuit connected between the outputs of the two data output buffers in each group, for making the outputs of the two data output buffer in each group the same level. Therefore, a data output speed of the data output buffer could be improved and the peak current could be also reduced.